SLM21814

600V High and Low Side Driver

PRODUCT SUMMARY

- V_{OFFSET} 600 V max.
- I_O+/- 4A / 4A
- V_{OUT} 10 V - 20 V
- $t_{on/off}$ (typ.) 170ns / 170ns

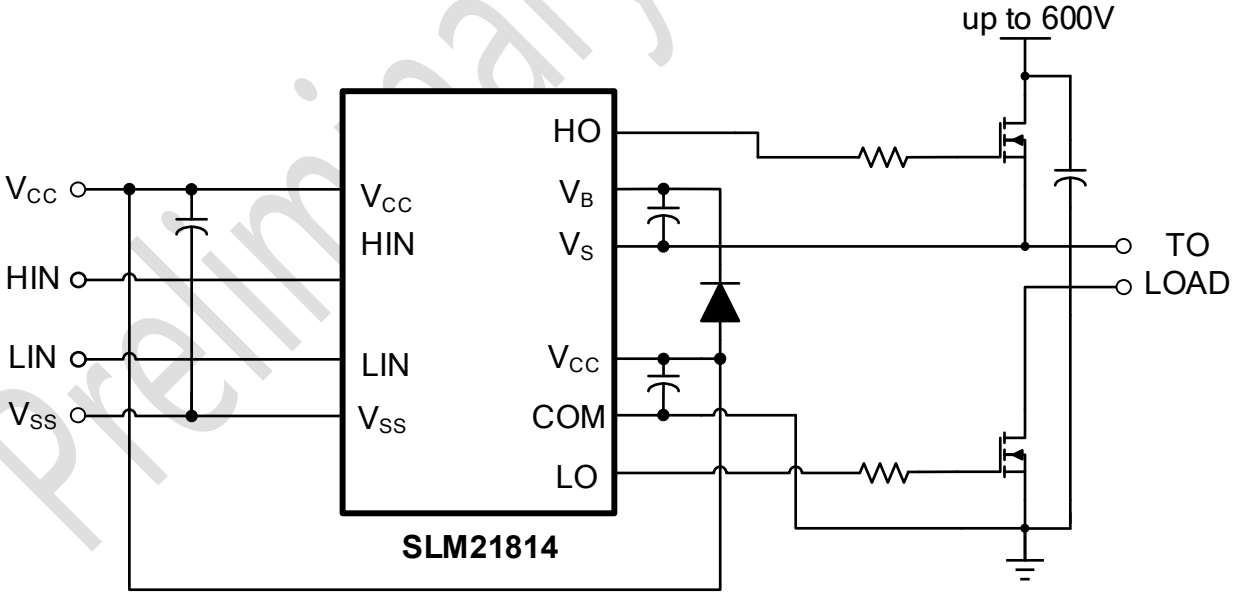
FEATURES

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Low V_{CC} operation
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V, and 5 V logic compatible
- CMOS Schmitt-triggered inputs with pull-down
- Matched propagation delay for both channels
- Outputs in phase with inputs
- RoHS compliant
- SOIC-8 package

GENERAL DESCRIPTION

The SLM2181 is a high voltage, high speed power MOSFET and IGBT drivers with independent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

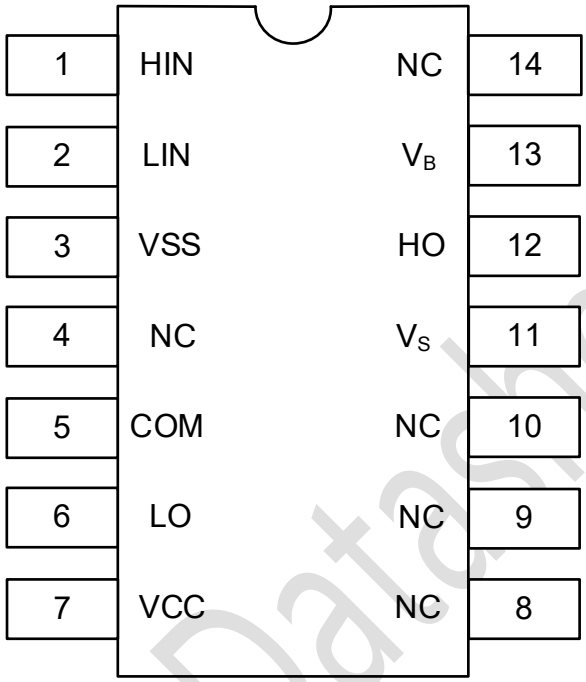
TYPICAL APPLICATION CIRCUIT



(Refer to Lead Assignments for correct configuration). This diagram shows electrical connections only.

Typical Application Circuit

PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOIC-14	

PIN DESCRIPTION

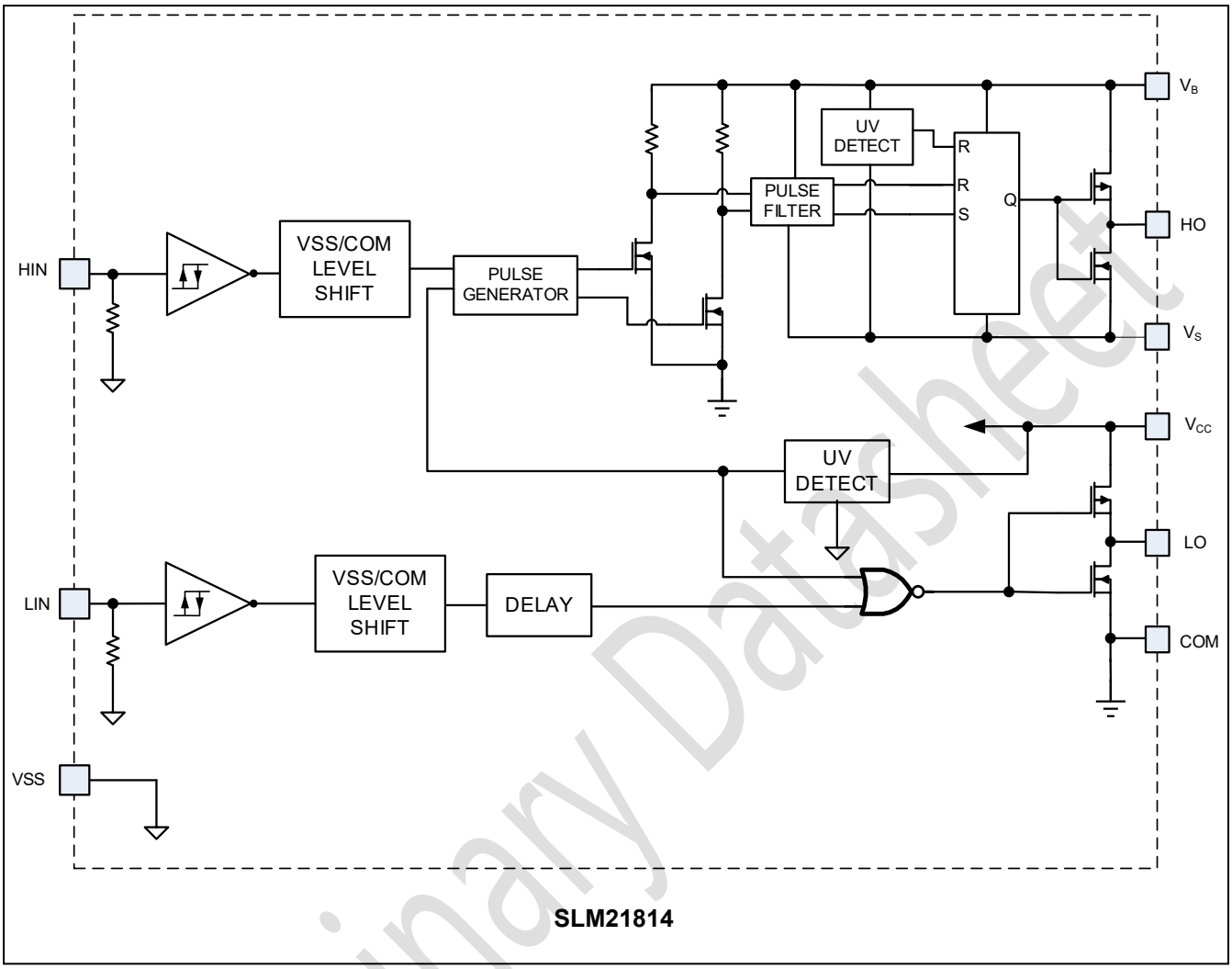
No.	Pin	Description
1	HIN	Logic input for high-side gate driver output (HO), in phase
2	LIN	Logic input for low-side gate driver output (LO), in phase
3	VSS	Logic ground
5	COM	Low-side return
6	LO	Low-side gate drive output
7	V_{CC}	Low-side and logic fixed supply
11	V_S	High-side floating supply return
12	HO	High-side gate drive output
13	V_B	High-side floating supply
4,8,9,10, 14	NC	No Connection

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
SLM21814CA-DG	SOIC14, Pb-Free	2500/Reel
SLM21814CA-TG	SOIC14, Pb-Free	100/Tube

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Definition		Min.	Max.	Units
V_B	High-side floating absolute voltage		-0.3	625	V
V_S	High-side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High-side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low-side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low-side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & $\overline{LIN}$)		-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		---	50	V/ns
P_D	Package power dissipation @ $T_A \leqslant +25°C$	PDIP-8	---	1.0	W
		SOIC-8	---	0.625	
Rth_{JA}	Thermal resistance, junction to ambient	PDIP-8	---	125	°C/W
		SOIC-8	---	200	
T_J	Junction temperature		---	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		---	300	

Note:
Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

RECOMMENDED OPERATIONG CONDITIONS

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating absolute voltage	V_S + 10	V_S + 20	V
V_S	High-side floating supply offset voltage	Note 1	600	
V_{HO}	High-side floating output voltage	V_S	V_B	
V_{CC}	Low-side and logic fixed supply voltage	10	20	
V_{LO}	Low-side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & LIN)	COM	V_{CC}	
T_A	Ambient temperature	- 40	125	°C

Note:
The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at a 15 V differential.

DYNAMIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15 V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on propagation delay	V_S = 0 V	---	130	160	ns
t_{off}	Turn-off propagation delay	V_S = 0V	---	120	150	
t_r	Turn-on rise time		---	25	35	
t_f	Turn-off fall time		---	17	25	
MT	Delay matching, HS & LS turn-on/off		---	---	10	

STATIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15 V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to COM and are applicable to all three logic input leads: HIN and LIN. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Logic “1” input voltage	V_{CC} = 10 V to 20V	2.5	---	---	V
V_{IL}	Logic “0” input voltage		---	---	0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 20 mA	---	---	1.4	
V_{OL}	Low level output voltage, V_O		---	0.02	0.15	
I_{LK}	Offset supply leakage current	V_B = V_S = 600 V	---	---	50	µA
I_{QBS}	Quiescent V_{BS} supply current	V_{IN} = 0 V	20	75	130	
I_{QCC}	Quiescent V_{CC} supply current		160	220	300	
I_{IN+}	Logic “1” input bias current	HIN=LIN = 5V	---	5	20	
I_{IN-}	Logic “0” input bias current	HIN=LIN= 0V	---	---	5	
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold		8.0	8.9	9.8	V
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold		7.4	8.2	9.0	
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold		8.0	8.9	9.8	V
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold		7.4	8.2	9.0	
I_{O+}	Output high short circuit pulsed current	V_O = 0 V V_{IN} = Logic “1” PW ⩽ 10 µs		4		A
I_{O-}	Output low short circuit pulsed current	V_O = 15 V V_{IN} = Logic “0” PW ⩽ 10 µs		4		

Switching and Timing Relationships

The relationships between the input and output signals of the SLM21814 are illustrated below in Figures 1, 2. From these figures, we can see the definitions of several timing parameters (i.e., t_{ON}, t_{OFF}, t_R, and t_F) associated with this device.

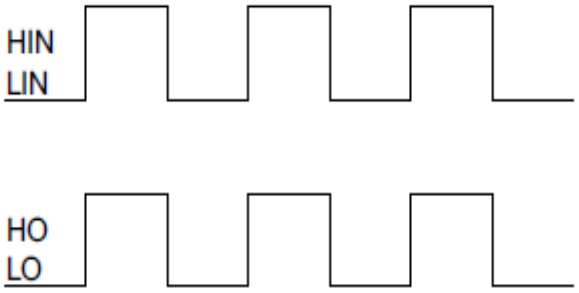


Figure 1. Input/Output Timing Diagram

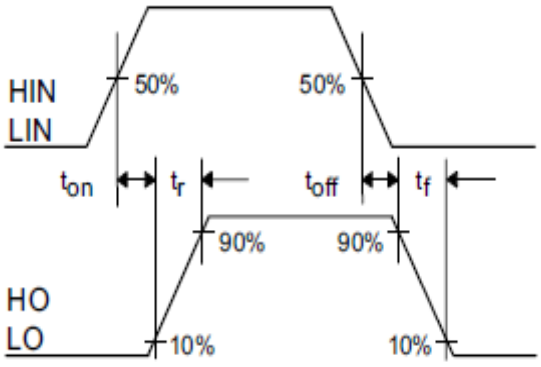


Figure 2. Switching Time Waveform Definitions

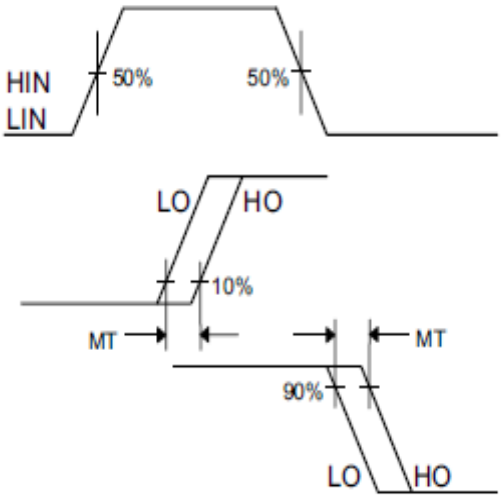
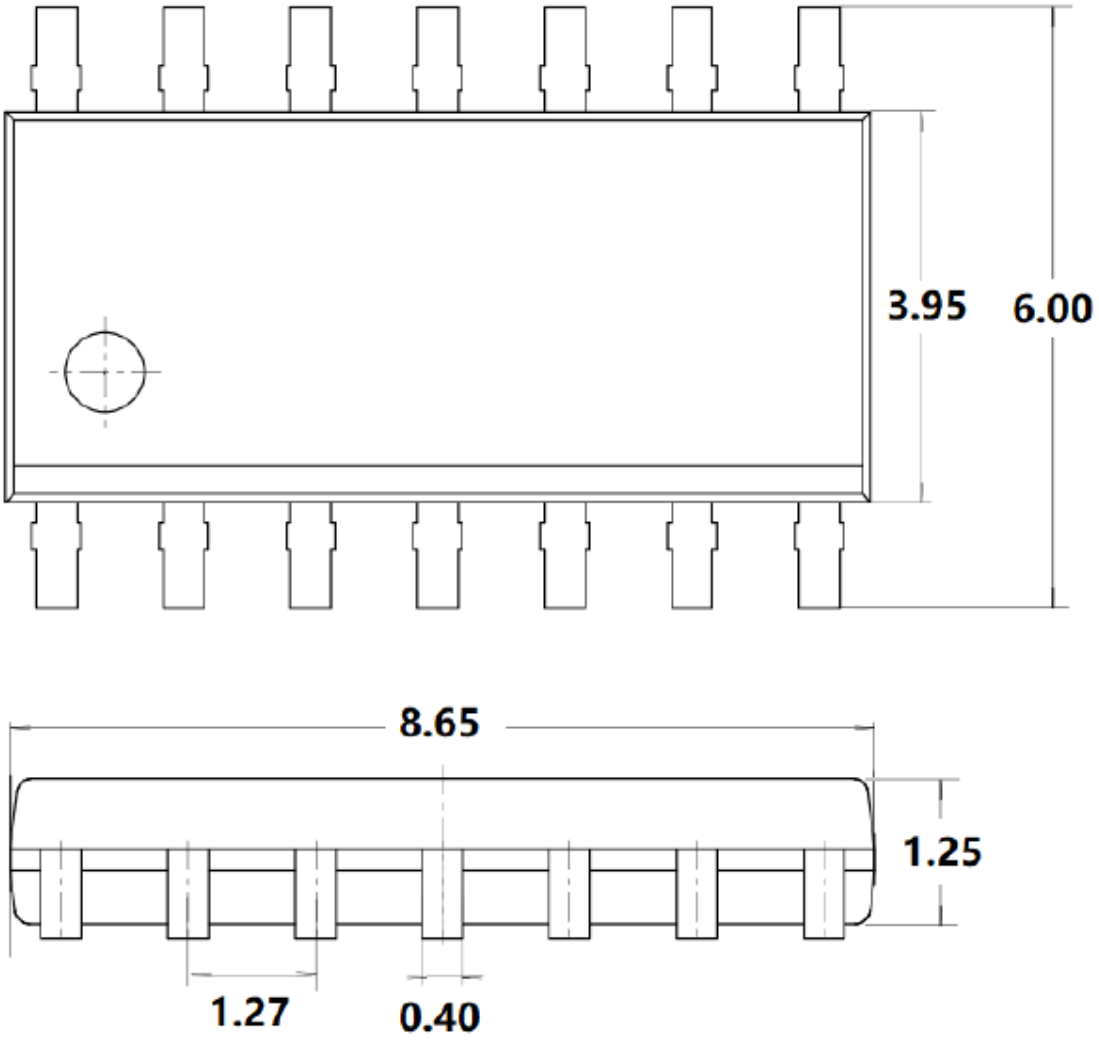


Figure 3. Delay Matching Waveform Definitions

PACKAGE CASE OUTLINES



Dimension Unit : mm

Revision History

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 0.1 datasheet, 2020-9-10	
Whole document	Draft datasheet released